

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Morishita, Y.

JC808 U.S. PTO
 09/619669
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Serial No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

Filing Date: Concurrently Herewith

Examiner: Unknown

For: AN INPUT/OUTPUT PROTECTION DEVICE FOR A SEMICONDUCTOR
INTEGRATED CIRCUIT

#3 / IDS
2-14-01
R. Stokes

Assistant Commissioner of Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

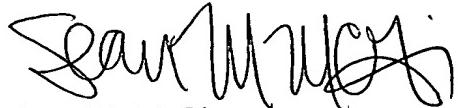
Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following documents listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents are provided herewith for the convenience of the Examiner. In compliance with the concise explanation requirement under 37 CFR §1.98(a)(3), the relevance of these documents are discussed on page 1 of the subject application.

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0481.

Respectfully submitted,



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Date: 7/19/00

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